REMARKS

An Excess Claim Fee Payment Letter, and corresponding excess claim fee, is submitted herewith for three (3) excess independent claims. Additionally, Applicant concurrently files herewith a Petition for Extension of Time, and corresponding extension of time fee, for a one-month extension of time.

Claims 1-18 remain pending in the application. Claims 1 and 4 have been amended to more particularly define the invention.

The indication of allowable subject matter in claims 8-10 and 15-17 is noted with appreciation. Claims 8, 10, 15, and 17 have been amended to independent form, making claims 8-10 and 15-17 allowable.

Further, Applicant respectfully submits that all the claims are allowable.

The Office Action states that claims 1-7, 11-14, and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art (APA) in view of Kurafuji, et al., United States Patent No. 6,584,528 and Virajpet, et al. United States Patent No. 6,480,948, and then states that claim 5 was rejected under 35 U.S.C. §103(a) as unpatentable over APA in view of Kurafuji, et al., Virajpet, et al., and Ueki et al, United States Patent No. 6,651,152. Thus, the exact basis for rejection of claim 5 is unclear. In any event, the rejections are respectfully traversed.

While the Office Action relies on Kurafuji, et al., in rejecting claims 1-7, 11-14, and 18, Kurafuji, et al. is not listed on the Notice of References Cited (Form PTO 892) which was a part of the Office Action and was not listed on any previous Notice of References Cited or in any Information Disclosure Statement in this application. It is requested that a Notice of References Cited be issued, listing Kurafuji so as to assure that it is properly of record in this

application.

THE CLAIMED INVENTION

The claimed invention is directed to microcomputer. In a first exemplary embodiment, as recited in claim 1 and illustrated in Figure 2 of the present application, the microcomputer 1 includes a central processing unit (CPU) 2, a cache 7, and a memory 12. A data bus 3 is connected to the CPU 2. A command bus 5 is connected to the CPU 2, the cache 7, and the memory 12. The command bus 5 is separated from the data bus 3, and the memory 12 is electrically isolated from the data bus 3.

In a second exemplary embodiment, as recited in claim 4 and also illustrated in Figure 2 of the present application, the microcomputer 1 includes a central processing unit (CPU) 2, a bus controller 4, a command cache 7, and a command memory 12. A first bus 3 electrically connects the bus controller 4 with the CPU 2. A second bus 5 electrically connects the command cache 7 with the CPU 2. A third bus 6 electrically connects the command cache 7 with the bus controller 4. A fourth bus 10 electrically connects the command memory 12 to the second bus 5. The second bus 5 is separated from the first bus 3, and the memory 12 is electrically isolated from the first bus 3.

THE PRIOR ART REFERENCES

The Admitted Prior Art

As depicted in Figure 1 of the present application, the APA discloses a microcomputer 41, including a central processing unit (CPU) 42, a bus controller 44, and a command cache 47. A first bus 43 connects the bus controller 44 with the CPU 42. A second bus 45 connects

the command cache 47 with the CPU 42. A third bus 46 connects the command cache 46 with the bus controller 44. The second bus 45 is separated from the first bus 43.

The Kurafuji et al. Reference

Kurafuji discloses a microprocessor. As depicted in Figure 1 of Kurafuji, the microprocessor P0 includes a processor core or processor (CPU) 1, a dedicated command memory 4, and a command/data memory 5. A command bus 7 is connected to the CPU 1 through a first unnumbered bus, a command fetch control unit 2, and a second unnumbered bus. The command bus 7 is also connected through a third unnumbered bus to the dedicated command memory 4. A data bus 8 is connected to the CPU 1 through a fourth unnumbered bus, a data access control unit 3, and a fifth unnumbered bus. The command bus 7 and the data bus 8 are connected to the command/data memory 5 through bus switches 12.

The Virajpet et al. Reference

Virajpet discloses a memory for storing an interrupt code.

The Ueki et al. Reference

Ueki discloses an external device controller and a SRAM.

ARGUMENT

In the invention as set for in claims 1-7, 11-14, and 18, the second or command bus is separated from the first or data bus. Further, the cache is electrically connected to a second memory (the second memory may, for example, correspond to the external memory 15

exemplariliy illustrated in Figure 2 of the Application.

The Examiner alleges that "command memory 4" and command/data memory 5" illustrated in Figure 1 of Kurafuji correspond to the "cache" and the "first memory/command memory" recited in claims 1 and 4 of the claimed invention, respectively.

However, the command memory 4, of Kurafuji, is not a "cache", because the fixed address is assigned to the command memory 4, as illustrated in Figures 7 and 8 of Kurafuji.

The claimed invention has a purpose of solving the problem caused by mis-hit in cache. Thus, the APA including a cache is not allowed to be combined with Kurafuji, which does not include a cache.

Since a cache is used to enable a CPU to access a memory at a high rate, the memory has to be electrically connected to the CPU through the cache. In order to maximize an efficiency of a cache, those skilled in the art would electrically connect all memories to the CPU through the cache.

Accordingly, if the APA including a cache is combined with Kurafuji, which does not include a cache, there would be obtained a circuit in which the bus 46 illustrated in Figure 1 of the Application is electrically connected to the command memory 4 of Kurafuji, and both of the data bus 43 and the bus 46, both illustrated in Figure 1 of the Application, are electrically connected to the command/data memory 5 of Kurafuji.

It is obvious that the resultant circuit is different in structure from the claimed invention in which the first memory 12 (or the command memory) is electrically connected to the command bus 5 (or the second bus) through which CPU 2 and the cache 7 are electrically connected to each other, as illustrated in Figure 2 of the Application.

Therefore, the claimed invention would not have been obvious in view of the cited

references.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-18, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including

extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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